# Ultra-shallow fluorine implantation from r.f. plasma as a method for improvement of electro-physical properties of MIS structures with PECVD gate dielectric layers

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## Introduction

In this work a comprehensive analysis of changes in electrical and reliability parameters, which are introduced by the presence of a fluorine-rich layer in the gate structure based on MOS ($Al/SiO_2/Si$) and MIS ($Al/SiO_xN_y/Si$) system, has been carried out. The surface of silicon substrates prior to the test structure execution was subjected to the processes of ultra-shallow ion implantation from $CF_4$ plasma, different, than those usually found in the literature. To this end, the conventional plasma reactors were utilized to carry out a plasma enhanced chemical vapour deposition process PECVD and reactive ion etching RIE. To perform gate dielectric layers the PECVD method was used. The conducted analysis of the electrical properties was complemented by spectroscopic measurements (SIMS), which allowed the identification of causes and effects of observed changes in electro-physical parameters.

## Experiment

To perform the test structures the NMOS technology with a non-self-aligned metal gate was selected. For the experiment the silicon plates type p were prepared with a crystal orientation <100> and resistivity of 4-10 Ωcm. The substrates cleaned using the RCA method were subject to the processes of manufacturing the passivating dielectric, which protects the silicon surface during the process of ultra-shallow implantation from the RF plasma. In the case of the structures with the gate dielectric in the form of silicon oxide ($SiO_2$), passivation was performed by high-temperature silicon oxidation process. The resulting thermal oxide thickness was about 15 nm. In the case of the structures with the gate dielectric in the form of silicon oxynitride ($SiO_xN_y$), the passivating oxide was prepared in PECVD process. The thickness of deposited oxide was about 7 nm. Then, the fluorine ion implantation process was carried out in $CF_4$ plasma through the passivating oxide. To carry out the process of implantation of fluorine the plasma reactors type PlasmaLab 80 + system manufactured by Oxford Instruments were utilized. To this end, both the reactor for carrying out dry etching process (RIE) and the reactor for plasma enhanced chemical vapour deposition process – PECVD were used.

*Table 1 Technological parameters of processes performed in the course of this work.*

| | Parameters of ultra-shallow fluorine implantation | | | | Layer deposition | | | | | | Ann. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $CF_4$ flow | Pressure | RIE power | PECVD power | Temp. | Pressure | Power | Gas flow | | | Temp. |
| | | | | | | | | $SiH_4$ | $N_2O$ | $NH_3$ | |
| | [ml/min] | [mTorr] | [W] | | [°C] | [mTorr] | [W] | [ml/min] | | | [°C] |
| $SiO_2$ | 50 | 200 | 160 | | 350 | 600 | 10 | 70 | 120 | - | 1100 |
| $SiO_xN_y$ | | | 80 | | | 500 | | 150 | 24 | 32 | |

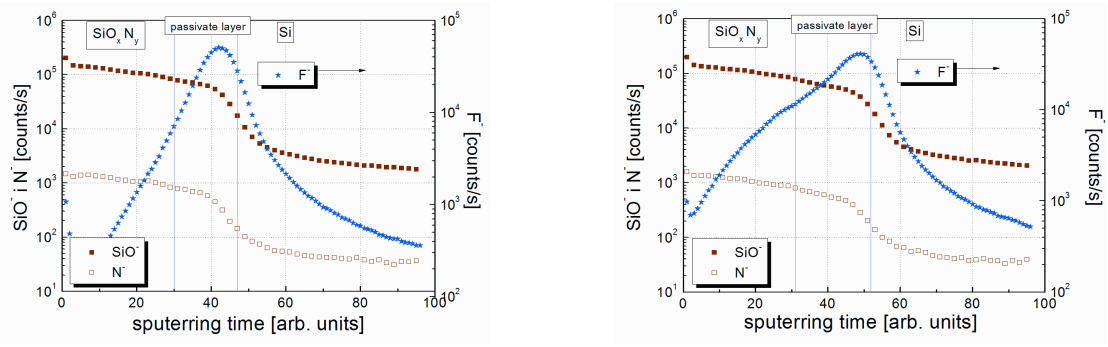
In the next technological step the layers of gate dielectrics, $SiO_2$ (13 nm) and $SiO_xN_y$ (7 nm), were deposited by PECVD method on the passivating layer generated on the surface in the result of the ultra-shallow implantation process. In addition, the structures with gate dielectrics were made, which were subjected to high-temperature annealing process in a standard quartz furnace under Ar atmosphere at

1100 °C for 30 min. This experiment allowed to check the thermal stability of fluorine in the gate dielectric/passivating layer/silicon structure. Additionally, the reference structures without modifying the silicon substrate in a $CF_4$ plasma were prepared. All parameters of the performed technological processes are specified in Table 1.

Ellipsometry measurements were carried out immediately after technological processes. The thicknesses of the layers obtained were measured using a single-wavelength ellipsometer ($\lambda$ = 632.8 nm). The analysis of spectroscopic measurements SIMS (Secondary Ion Mass Spectroscopy) was also carried out, which allowed to determine the chemical composition and the profiles of distribution of fluorine atoms in the resulting structures.

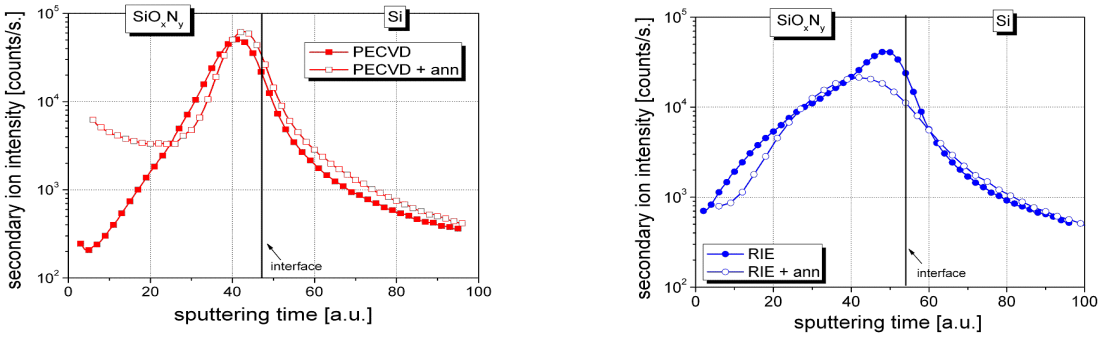
## *The results obtained from spectroscopic measurements (SIMS)*

Application of plasma deposition technology PECVD to form the gate dielectric layer ($SiO_2$ or $SiO_xN_y$) on the passivating layer generated by ultra-shallow implantation from $CF_4$ plasma, leads to the formation of the system of following layers: gate dielectric layer/passivating layer/silicon [12].




a) b)

Fig. 1 Comparison of $SiO^-$, $N^-$ and $F^-$ profiles within the silicon oxynitride layers after modification of silicon substrate in PECVD (a) and RIE (b) reactor.




a) b)

Fig. 2 Thermal stability of fluorine concentration within the $SiO_xN_y$ layers after modification of silicon substrate in PECVD (a) and RIE (b) reactor.

Figure 1 shows the comparison of profiles of fluorine, nitrogen and oxide phase in the layer of silicon oxynitride after modification of the silicon substrate surface in PECVD (Figure 1a) and RIE (Figure 1b) reactors. Analysis of the profiles indicates that, regardless of the type of reactor, in which the process of ultra-shallow implantation of fluorine ions from RF plasma was carried out, the maximum concentration of fluorine differs insignificantly. It is worth mentioning that the construction of both plasma reactors is essentially different. The main difference is the different geometry of the electrodes, which has a significant impact on the energy and density of ions in the RF plasma. The maximums of the concentration of fluorine in case of silicon oxynitride, are located very close to the semiconductor / passivating layer (rich in fluorine) interface. Only in the case of silicon surface modification in the RIE

reactor, you may notice the increased concentration of fluoride in the volume of the gate dielectric layer, in relation to the concentration of fluoride in the layer modified in the PECVD reactor. Figure 2 shows the comparison of the profiles of fluorine atoms before and after the high temperature annealing of dielectric layers. As is apparent from the profiles presented in Figure 2, in contrast to the results described in other papers connected with implantation of fluorine [eg 13]the fluorine from the passivating layer, covered with a layer of plasma-deposited $SiO_xN_y$ is thermally stable. Fluorine atoms under the influence of the structure annealing at 1100 °C are not removed from it. What's more, it seems that the dose of fluorine deposited at the interface after annealing is very similar to the dose before annealing. There are very small changes: under the influence of high temperature of the process the fluorine concentration value at the maximum of its distribution, in the case of modification at the PECVD reactor slightly increases, and for modifications in the RIE reactor - slightly diminishes (see Figure 2a and 2b). In the case of the plasma silicon oxide layer, the obtained results are very similar to those obtained for $SiO_xN_y$ layers. This is confirmed by fluorine profiles shown in Figure 3. It may be noted that the high temperature (1100 °C) annealing of silicon oxide layer does not affect significantly the value of the maximum concentration of fluoride.

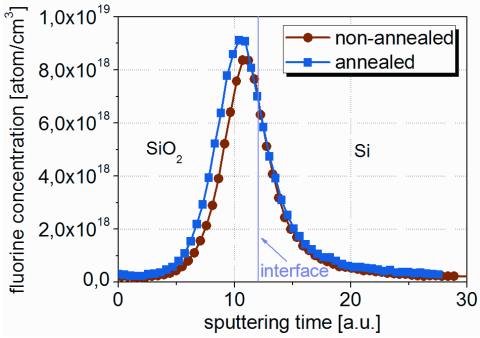
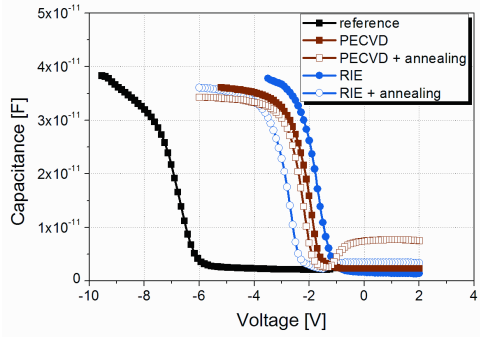
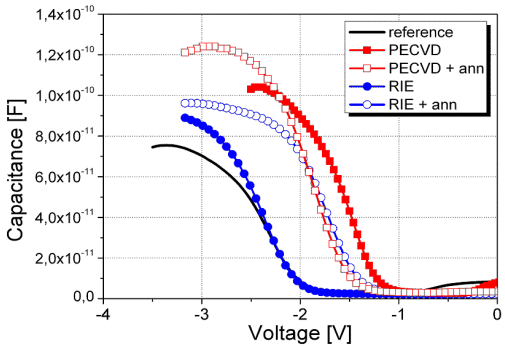



*Fig. 3 Thermal stability of fluorine concentration within the SiO2 layer after modification of silicon substrate.*

## *The analysis of electrical characteristics of MOS (MIS) test structures with gate dielectrics produced by PECVD method.*

Figures 4a-b show the comparison of the C-V characteristics (1 MHz) obtained for the MOS capacitors (Fig. 4a) with the gate dielectric in the form of silicon oxide, and MIS (Fig. 4b) with the gate dielectric in the form of silicon oxynitride ($SiO_xN_y$), after the silicon surface modification processes in reactors for PECVD and RIE. For comparison, the drawings show also the characteristics of MOS and MIS reference structures.




a) b)

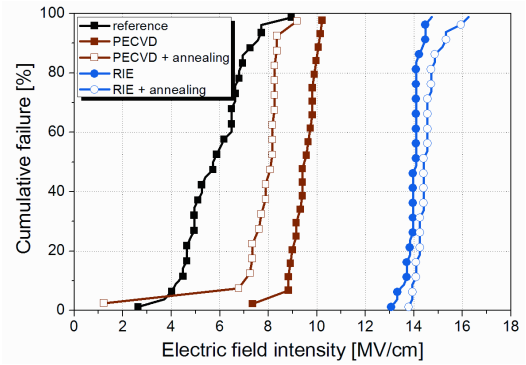
Fig. 4a Comparison of C-V characteristics of a) MOS structures; b) MIS structures, fabricated on modified silicon substrates; C-V characteristics of reference structure was also shown.

The analysis of the capacitance-voltage (C-V) characteristics of the prepared MOS (MIS) test structures has shown that the systems: semiconductor/passivating layer/gate dielectric produced on the modified silicon substrates, are characterized by smaller values (in absolute value) of flat-band voltages ($U_{FB}$) and effective load (Qeff) compared to the reference structures. However, the density of surface states in the middle of the silicon forbidden energy band ($D_{itmb}$) does not change significantly (see Table 2). The introduction of fluorine in the interface area of MOS (MIS) structures also results in the slight reduction of the electric permittivity of dielectric layers produced by PECVD, which can be utilized in the technology of intermetallic layers of integrated circuits.

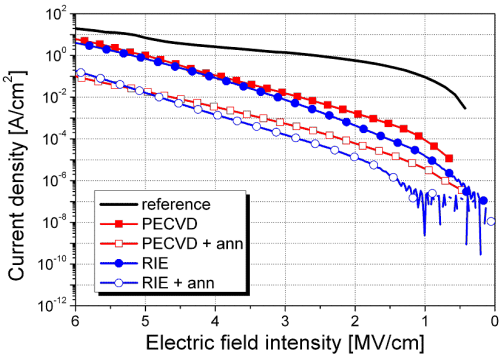
*Table 2 Basic electro-physical properties of PECVD silicon dioxide and PECVD $SiO_xN_y$ (in the brackets) layers.*

| | reference | PECVD | PECVD + ann. | RIE | RIE + ann. |
|---|---|---|---|---|---|
| thickness [Å] | 130 (70) | 122 (46) | 108 (42) | 156 (61) | 130 (54) |
| electric permittivity | 3,8 (4,3) | 3,3 (3,9) | 2,8 (4,2) | 4,6 (4,5) | 3,5 (4,1) |
| $D_{itmb}$ [$ev^{-1}cm^2$] | 3,2 x $10^{12}$ (6,3 x $10^{12}$) | 3,2 x $10^{12}$ (8,7 x $10^{12}$) | 3 x $10^{12}$ (9 x $10^{12}$) | 5 x $10^{12}$ (6,7 x $10^{12}$) | 4,6 x $10^{12}$ (7 x $10^{12}$) |
| $Q_{eff}/q$ [$cm^{-2}$] | 7,9 x $10^{12}$ (4,2 x $10^{12}$) | 1,8 x $10^{12}$ (3,4 x $10^{12}$) | 1,5 x $10^{12}$ (3 x $10^{12}$) | 8,6 x $10^{12}$ (4,1 x $10^{12}$) | 2,6 x $10^{12}$ (2,6 x $10^{12}$) |

The analysis of current-voltage characteristics (I-V) (see Figure 5a and 5b) of MOS and MIS test structures showed that the structures produced on the substrates, which have been subjected to the processes of fluorine implantation from $CF_4$ plasma, are characterized by dramatically increasing uniformity of breakdown voltage.




*a)*




*b)*

Fig. 5 Cumulative failure of a) MOS structures; b) MIS structures, investigated in the course of this work

# Results

Based on the technological experiments and spectroscopic measurements (SIMS) carried out in this work it was stated clearly that the processes of ultra-shallow implantation of fluorine ions from $CF_4$ plasma, performed in the classical plasma reactors (PECVD and RIE), are ideal for surface modification of silicon substrates by introducing a high concentration of fluoride into their subsurface area.

The results of this study show that the developed technology of ion implantation of fluorine in $CF_4$ plasma can be safely used in self-aligned CMOS technology, as well as in technology with extremely low thermal budget, such as on strained substrates (SiGe).

# Bibliografia

[1] M. Kalisz et al., Vacuum 2008, 82: 1040-1045; [2] Endo K, T. Tatsumi, J Appl Phys 1995, 78:1370; [3] M. Kalisz et al., J Telecomm Inf Technol 2007, 2-3: 5-9